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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,480	09/28/2001	Keiichi Fujimoto	740819-653	2785

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EXAMINER

PATEL, PARESH H

ART UNIT PAPER NUMBER

2829

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/964,480

Applicant(s)

FUJIMOTO ET AL.

Examiner

Paresh Patel

Art Unit

2829

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 September 2001.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION***Drawings***

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the interconnect substrate from deforming as claimed in claims 1 and 7; and a mechanism which applies pressing force to all of said dummy isolated patterns of claims 6 and 12 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

The drawings are objected to under 37 CFR 1.83(a) because they fail to show interconnect substrate from deforming toward the wafer tray as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to

Art Unit: 2829

reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Regarding claims 1 and 7, limitation "a plurality of protrusions ... for preventing said interconnect substrate from deforming toward said wafer tray when an internal pressure of said sealed space is reduced" wherein deforming the interconnect substrate is not clear because drawing does not support this. Also if there is reduction in pressure in sealed space 118, elastic sheet 103 will deform first, (before deforming the interconnect substrate) which will cause problems as defined in prior art (JP 11-135582). Specification also fails to disclose this problem because elastic sheet is laid between wafer tray and interconnect substrate.

Regarding claims 1 and 7, limitation "an elastic sheet held on said interconnect substrate at a periphery thereof" wherein specification fails to support this limitation. The elastic sheet is also held at rubber sheet 110, and hence claimed structure of testing system differ from disclosure.

Regarding claims 5 and 11, both claim and specification fails to disclose the use of dummy isolated pattern.

Claims 2-4, 6, 8-10 and 12 are rejected because they depend from rejected claims.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Art Unit: 2829

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1 and 7, it is not clear who/what reduces internal pressure of test system.

Regarding claims 6 and 12, it is not clear that who/what applies pressing force to all of said dummy isolated patterns.

All dependent claims are rejected.

Claim Objections

Claim 12 is objected to because of the following informalities: "Claim 7" should read -Claim 11-. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

Art Unit: 2829

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakata et al. (US 6297658).

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Nakata et al. (hereafter Nakata) in fig. 1 discloses: a semiconductor integrated circuit testing system for testing electric characteristics of a plurality of semiconductor integrated circuit devices formed on a semiconductor wafer in the lump, comprising:

a wafer tray [11] for holding said semiconductor wafer [10];

an interconnect substrate [13] facing said semiconductor wafer held by said wafer tray and having interconnect layers [20] to which a testing voltage is externally input [lines 1-7 of column 2];

a ring-shaped sealing member [14] provided between said wafer tray and said interconnect substrate for forming a sealed space [15 and 25] together with said wafer tray and said interconnect substrate;

an elastic sheet [12] held on said interconnect substrate at a periphery thereof [see end of 12 with 13];

a plurality of probe terminals [17] provided on said elastic sheet in positions respectively corresponding to external electrodes [16] of said plurality of semiconductor integrated circuit devices [chips of 10] and electrically connected to said interconnect layers [19]; and

a plurality of protrusions [17 at the end of 21] protruding toward said wafer tray and provided on said elastic sheet for preventing said interconnect substrate from deforming toward said wafer tray when an internal pressure [via 22] of said sealed space is reduced.

Regarding claims 2 and 8, Nakata discloses: said plurality of protrusions are disposed in a region on said elastic sheet where said plurality of probe terminals are distributed relatively sparsely [lines 40-64 of column 2].

Regarding claims 3 and 9, Nakata discloses: said plurality of protrusions are disposed in a region on said elastic sheet outside a region where said plurality of probe terminals are provided [lines 40-64 of column 2].

Regarding claims 4 and 10, Nakata discloses: said plurality of protrusions are arranged circumferentially in a region on said elastic sheet corresponding to a periphery of said semiconductor wafer [lines 40-64 of column 2].

Regarding claims 5 and 11, Nakata discloses: said plurality of probe terminals are composed of electrically connecting isolated patterns provided on a first face [face of 12 facing 13] of said elastic sheet facing said interconnect substrate and electrically connected to said interconnect layers, and bumps [17] respectively integrated with said electrically connecting isolated patterns and provided on a second face [face of 12 facing 10 or 11] of said elastic sheet facing said wafer tray [11], and said plurality of protrusions are composed of dummy isolated patterns [19] provided on the first face of said elastic sheet, and dummy bumps [17] respectively integrated with said dummy isolated patterns and provided on the second face of said elastic sheet.

Regarding claims 6 and 12, Nakata discloses: a pressing force applied to all of said dummy isolated patterns [inherent to 22 and lines 8-13 of column 2] when the internal pressure of said sealed space is reduced is **approximately 1/3 or more** of a pressing force applied to all of said electrically connecting isolated patterns when the internal pressure of said sealed space is reduced [lines 1-14 of column 3].

Regarding claim 7, Nakata discloses: a semiconductor integrated circuit testing method using a testing system including a wafer tray for holding a semiconductor wafer on which a plurality of semiconductor integrated circuit devices respectively having external electrodes are formed; an interconnect substrate having interconnect layers to which a testing voltage is externally input; a ring-shaped sealing member provided

between said wafer tray and said interconnect substrate for forming a sealed space together with said wafer tray and said interconnect substrate; an elastic sheet held on said interconnect substrate at a periphery thereof; a plurality of probe terminals provided on said elastic sheet in positions respectively corresponding to said external electrodes of said plurality of semiconductor integrated circuit devices and electrically connected to said interconnect layers; and a plurality of protrusions protruding toward said wafer tray and provided on said elastic sheet, the method comprising the steps of:

holding said semiconductor wafer [10] on said wafer tray [11] with said external electrodes [16] of said plurality of semiconductor integrated circuit devices [chips of 10] respectively facing said plurality of probe terminals [17] provided on said elastic sheet [12];

forming said sealed space [15 and 25] with said wafer tray, said ring-shaped sealing member [14] and said interconnect substrate [13] by making said wafer tray holding said semiconductor wafer and said interconnect substrate come close to each other [lines 64-67 of column 6 and lines 1-21 of column 7];

reducing an internal pressure [lines 35-42 of column 7] of said sealed space for bringing said plurality of probe terminals into contact with said external electrodes respectively facing said plurality of probe terminals; and

testing electric characteristics of said plurality of semiconductor integrated circuit devices in the lump by applying the testing voltage to said external electrodes in contact with said plurality of probe terminals through said interconnect layers and said plurality of probe terminals [lines 1-7 of column 2], wherein the step of reducing the internal

Art Unit: 2829

pressure of said sealed space includes a sub-step of preventing said interconnect substrate from deforming toward said wafer tray by bringing said plurality of protrusions into contact with said semiconductor wafer held on said wafer tray [inherent to 17 of 12].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on M-F (8:30 to 4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703-308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



**KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800**

Paresh Patel
March 25, 2003